

## AMENDMENTS TO THE CLAIMS

1           1.       (Original)     A data processor for use in a wireless communication device,  
2 comprising:  
3           a processing unit;  
4           an instruction pipeline circuit;  
5           at least one processing module;  
6           a timer for generating a time-out interval; and  
7           power control logic for detecting a sleep instruction and placing the processing unit,  
8 instruction pipeline circuit and at least one processing module in a low-power state, where  
9 the power control logic is operative in response to a wake-up signal to reactivate the  
10 instruction pipeline circuit, and consequently at least one processing module only to the  
11 extent required by the wake-up signal.

1           2.       (Original)     The processor of claim 1, where the instruction pipeline circuit  
2 comprises a multi-stage instruction pipeline circuit.

1           3.       (Original)     The processor of claim 1, where the wake-up signal comprises  
2 a logical OR combination of one or more predetermined wake-up conditions and the time-out  
3 interval.

1           4.       (Original)     The processor of claim 1, where the power control logic  
2 comprises instruction decode logic to detect the sleep instruction.

1           5.       (Original)     The processor of claim 1, where the power control logic  
2 comprises branch condition logic to respond to the wake-up signal.

1           6.       (Original)     The processor of claim 1, where the power control logic,  
2 having specified one or more wake-up conditions that the processing unit will respond to  
3 when in a low-power state, generates the wake-up signal upon detecting the one or more  
4 wake-up conditions or the time-out interval.

1           7.       (Original)     The processor of claim 1, where the power control logic  
2     instructs the instruction pipeline circuit to complete any instructions preceding the sleep  
3     instruction.

1           8.       (Original)     The processor of claim 7, where the power control logic  
2     instructs the instruction pipeline circuit to cease fetching new instructions after encountering  
3     a sleep instruction whose wake-up conditions are currently deasserted.

1           9.       (Original)     The processor of claim 1, wherein the processing unit,  
2     instruction pipeline circuit and at least one processing module are formed together on a  
3     common silicon substrate using CMOS processing.

1           10.      (Original)     The processor of claim 6, wherein the wake-up conditions and  
2     time-out interval are stored in a register by the power control logic.

1           11.      (Currently Amended) An article of manufacture having at least one computer  
2     readable medium encoded with a computer program comprising ~~recordable medium having~~  
3     ~~stored thereon~~ executable instructions and data which, when executed by at least one  
4     processing device, cause the at least one processing device to:  
5         detect a sleep instruction for the processing device;  
6         specify one or more wake-up conditions and a time-out interval;  
7         power down an instruction pipeline and one or more processor modules;  
8         reactivate the instruction pipeline upon detection of a wake-up signal corresponding  
9     to either a wake-up condition or the time-out interval, and  
10        process one or more instructions in the instruction pipeline to reactivate any of the  
11     one or more processor modules required to respond to a detected wake-up condition.

1           12.      (Original)     The article of manufacture of claim 11, wherein the processing  
2     device executes any instructions received by the instruction pipeline before the sleep  
3     instruction is received.

1           13.     (Original)     The article of manufacture of claim 11, wherein the instruction  
2 pipeline comprises a multistage instruction pipeline, and the processing device reactivates  
3 only stages in the multistage instruction pipeline and/or the function units needed to process  
4 one or more instructions necessary to analyze and respond to the wake-up signal.

1           14.     (Original)     The article of manufacture of claim 11, further comprising a  
2 register for holding the specified wake-up conditions and time out signal.

1           15.     (Original)     The article of manufacture of claim 11, where the processing  
2 device is implemented as part of a single-chip wireless communication device.

1           16.     (Original)     The article of manufacture of claim 11, where the executable  
2 instructions and data comprise control logic for controlling the operation of the processing  
3 device.

1           17.     (Original)     The article of manufacture of claim 11, where the processing  
2 device powers down the one or more processor modules by freezing a clock signal for said  
3 one or more modules.

1           18.     (Original)     The article of manufacture of claim 11, where the processing  
2 device powers down the one or more processor modules by placing said one or more  
3 modules in an idle mode.

1           19.     (Currently Amended) A method for managing power in a communications  
2 processor by selectively removing one or more processor modules from a standby mode,  
3 comprising:

4           storing one or more wake-up conditions and a time-out interval in a register;  
5           receiving a processor sleep instruction;  
6           executing any pending instructions received by the processor before the sleep  
7 instruction;

8            powering down the one or more processor modules, where one of the processor  
9 modules comprises an instruction pipeline circuit;

10           receiving a processor wake-up signal corresponding to one of said wake-up  
11 conditions or said time-out interval;

12           powering up only the processor modules required to respond to the detected processor  
13 wake-up signal.

1           20.     (Currently Amended) The method of claim 19, wherein one of the ~~processor-~~  
2 ~~modules comprises an~~ instruction pipeline circuit comprises a plurality of instruction pipeline  
3 stages.